

CLAIMS

What is claimed is:

- 1 1. A write select circuit comprising:
 - 2 a pulse stretcher stretching clock pulses;
 - 3 a READ/WRITE decode selectively passing stretched said clock pulses responsive to a write select signal; and
 - 5 a write driver receiving passed said stretched clock pulses and driving said write select pulses responsive to received said stretched clock pulses.
- 1 2. A write select circuit as in claim 1, wherein said write select circuit is a CMOS write select circuit and said pulse stretcher comprises:
 - 3 a delay receiving a local clock and passing a delayed clock; and
 - 4 a NAND gate receiving said local clock and said delayed clock and providing stretched said clock pulses.
- 1 3. A CMOS write select circuit as in claim 2, wherein said NAND gate is a 2 input NAND gate and said delay is a group of series connected inverters.
- 1 4. A write select circuit as in claim 1, wherein said write select circuit is a CMOS write select circuit and said READ/WRITE decode is a dynamic decode comprising:
 - 3 a pair of series connected complementary field effect transistors (FETs), stretched said clock pulses being connected to the gates of said pair, a common drain connection of said pair being a READ/WRITE decode output; and
 - 6 at least one write enable FET, selectively providing a path to ground for said pair.

1 5. A CMOS write select circuit as in claim 4, wherein said write driver comprises:
2 a pseudo latch P-type FET (PFET), said READ/WRITE decode output being
3 connected to a conductive terminal of said pseudo latch PFET; and
4 a first inverter, said READ/WRITE decode output being an input to said first
5 inverter.

1 6. A CMOS write select circuit as in claim 5, said write driver further comprising a
2 second inverter driving said write select pulses, an output of said first inverter being an
3 input of said second inverter.

1 7. A bit decoder comprising:
2 a pulse stretcher stretching clock pulses;
3 a bit decode selectively passing stretched said clock pulses responsive to a column
4 address; and
5 a column driver receiving passed said stretched clock pulses and driving said
6 column select pulses responsive to received said stretched clock pulses.

1 8. A bit decoder as in claim 7, wherein said bit decoder is a CMOS bit decoder and
2 said pulse stretcher comprises:
3 a delay receiving a local clock and passing a delayed clock; and
4 a NAND gate receiving said local clock and said delayed clock and providing
5 stretched said clock pulses.

1 9. A CMOS bit decoder as in claim 8, wherein said NAND gate is a 2 input NAND
2 gate and said delay is a group of series connected inverters.

1 10. A bit decoder as in claim 7, wherein said bit decoder is a CMOS bit decoder and
2 said bit decode is a dynamic decode comprising:

3 an n bit address decode connected between a decode node and a common source
4 node;

5 a restore FET connected between a supply and said decode node;
6 a complementary pair of enable FETs, a first of said complementary pair being
7 connected between said supply and a decode out of said bit decode, a second of said
8 complementary pair being connected between a supply return and said common source
9 node, the gate of said restore FET and of each of said complementary pair being
10 connected to an output of said pulse stretcher;

11 a decode out FET connected between said decode out and said enable node, said
12 decode node being connected to the gate of said decode out FET; and

13 a first pseudo latch FET connected between said supply and said decode node and
14 gated by said decode out.

1 11. A CMOS bit decoder as in claim 10, wherein said write driver comprises:
2 a second pseudo latch FET connected between said supply and said decode out;
3 and

4 a decode out inverter driving said column select pulses and connected to the gate
5 of said second pseudo latch FET, said decode out being an input to said decode out
6 inverter.

1 12. A CMOS bit decoder as in claim 11, wherein each of said decode out FET and
2 said second of said complementary pair are N-type FETs and each of said restore FET,
3 said first of said complementary pair, said first pseudo latch FET and said second pseudo
4 latch FET are P-type FETs.

1 13. A CMOS bit decoder as in claim 12, wherein said n-bit address decode comprises
2 n parallel NFETs connected between said decode node and said common source node and
3 said decode out inverter comprises a pair of parallel PFETs.

1 14. A random access memory (RAM) comprising:
2 a memory array comprising a plurality of memory cells organized as a plurality of
3 rows and columns;
4 a word decoder selecting a word line identifying one of said rows responsive to a
5 memory location access request;
6 a bit decoder providing column select pulses responsive to said memory location
7 access request;
8 a column select selecting a column responsive to said column select pulses; and
9 a write select selectively providing write select pulses, said write select pulses
10 being wider than corresponding said column select pulses.

1 15. A RAM as in claim 14, wherein said write select comprises:
2 a pulse stretcher stretching clock pulses;
3 a READ/WRITE decode selectively passing stretched said clock pulses
4 responsive to a write select signal; and
5 a write driver receiving passed said stretched clock pulses and driving said write
6 select pulses responsive to received said stretched clock pulses.

1 16. A RAM as in claim 15, wherein said RAM is a CMOS RAM and said
2 READ/WRITE decode is a dynamic decode comprising:
3 a pair of series connected complementary field effect transistors (FETs), stretched
4 said clock pulses being connected to the gates of said pair, a common drain connection of
5 said pair being a READ/WRITE decode output; and
6 at least one write enable FET, selectively providing a path to ground for said pair.

1 17. A CMOS RAM as in claim 16, wherein said write driver comprises:
2 a pseudo latch P-type FET (PFET), said READ/WRITE decode output being
3 connected to the drain of said pseudo latch PFET; and

4 a first inverter, said READ/WRITE decode output being an input to said first
5 inverter.

1 18. A CMOS RAM as in claim 17, said write driver further comprising a second
2 inverter driving said write select pulses, an output of said first inverter being an input of
3 said second inverter.

1 19. A RAM as in claim 15, wherein said bit decoder comprises:
2 a pulse stretcher stretching clock pulses;
3 a bit decode selectively passing stretched said clock pulses responsive to a column
4 address; and
5 a column driver receiving passed said stretched clock pulses from said bit decode
6 and driving said column select pulses responsive to received said stretched clock pulses.

1 20. A RAM as in claim 19, wherein said RAM is a CMOS RAM and said bit decode
2 is a dynamic decode comprising:
3 an n bit address decode connected between a decode node and a common source
4 node;
5 a restore FET connected between a supply and said decode node;
6 a complementary pair of enable FETs, a first of said complementary pair being
7 connected between said supply and a decode out of said bit decode, a second of said
8 complementary pair being connected between a supply return and said common source
9 node, the gate of said restore FET and of each of said complementary pair being
10 connected to an output of said pulse stretcher;
11 a decode out FET connected between said decode out and said enable node, said
12 decode node being connected to the gate of said decode out FET; and
13 a first pseudo latch FET connected between said supply and said decode node and
14 gated by said decode out.

1 21. A CMOS RAM as in claim 20, wherein said write driver comprises:
2 a second pseudo latch FET connected between said supply and said decode out;
3 and
4 a decode out inverter driving said column select pulses and connected to the gate
5 of said second pseudo latch FET, said decode out being an input to said decode out
6 inverter.

1 22. A CMOS RAM as in claim 21, wherein each of said decode out FET and said
2 second of said complementary pair are N-type FETs and each of said restore FET, said
3 first of said complementary pair, said first pseudo latch FET and said second pseudo latch
4 FET are P-type FETs.

1 23. A CMOS RAM as in claim 22, wherein said n-bit address decode comprises n
2 parallel NFETs connected between said decode node and said common source node and,
3 said decode out inverter comprises a pair of parallel P FETs.

1 24. A RAM as in claim 19, wherein each said pulse stretcher comprises:
2 a delay receiving a local clock and passing a delayed clock; and
3 a NAND gate receiving said local clock and said delayed clock and providing
4 stretched said clock pulses.

1 25. A RAM as in claim 24, wherein said delay in said write select is twice as long as
2 said delay in said bit decoder.

1 26. A RAM as in claim 25, wherein each said NAND gate is a 2 input NAND gate
2 and each said delay is a group of series connected inverters.

1 27. A RAM as in claim 25, wherein said column select pulses are wider than word
2 line pulses provided to said selected word line by said word decoder.

1 28. A RAM as in claim 27, wherein said plurality of memory cells are static RAM
2 (SRAM) cells.

1 29. A RAM as in claim 27, wherein said SRAM cells are 2 port SRAM cells.

1 30. A RAM as in claim 27, wherein said RAM is an SRAM macro on an integrated
2 circuit (IC) chip.

1 31. A CMOS integrated circuit (IC) chip including a static random access memory
2 (SRAM), said SRAM comprising:

3 an array comprising a plurality of SRAM cells organized as a plurality of rows
4 and columns;

5 a word decoder selectively providing a word line pulse to a word line selected
6 from one of said rows, said word line pulse being synchronized to a local clock, said
7 word decoder pulsing the selected said word line responsive to an access request;

8 a bit decoder comprising:

9 a pulse stretcher stretching clock pulses,

10 a bit decode selectively passing stretched said clock pulses responsive to a
11 column address, and

12 a column driver receiving passed said stretched clock pulses and driving a
13 column select pulse responsive to each received one of said stretched clock
14 pulses, said column select pulse being wider than a word line select pulse from
15 said word decoder;

16 a column select selecting a column responsive to said column select pulse; and
17 a write select comprising:

18 a pulse stretcher stretching clock pulses,

19 a READ/WRITE decode selectively passing stretched said clock pulses
20 responsive to a write select signal, and

21 a write driver receiving passed said stretched clock pulses from said
22 READ/WRITE decode and driving a write select pulse responsive to each
23 received one of said stretched clock pulses, each said write select pulse being
24 wider than said column select pulse.

- 1 32. A CMOS IC as in claim 31, wherein each said pulse stretcher comprises:
2 a delay receiving said local clock and passing a delayed said local clock, said
3 delay in said write select being longer than said delay in said bit decoder; and
4 a NAND gate receiving said local clock and providing said stretched clock pulses.

- 1 33. A CMOS IC as in claim 32, wherein each said NAND gate is a 2 input NAND
2 gate and each said delay is a group of series connected inverters.

- 1 34. A CMOS IC as in claim 33, wherein said delay in said write select is twice as
2 long as said delay in said bit decoder.

- 1 35. A CMOS IC as in claim 30, wherein said SRAM cells are 2 port SRAM cells.